UWB Using Programmable Logic

Tiago Costa*, Sérgio Reis Cunha† and José Carlos Alves‡

***Abstract*—This work will demonstrate a simple receiver and transmitter architecture, based on the Continuous-Time Binary-Value (CTBV) technique, to implement an Impulse-Radio Ultra-Wideband (IR-UWB) communication system in a Programmable Logic Device (in a Field-Programmable Gate Array, FPGA). It will also de demonstrated how the pulse generator and pulse detector designs were implemented and tested in FPGA hardware for two proof-of-concept scenarios: measurement of the propagation delay of a transmission line and line distance estimation, and also board-to-board transceiver operation.**

***Index Terms*—CTBV; FPGA; IR-UWB; Ranging measurements.**

I. Introduction

In 2002 the FCC approved the usage of parts of the RF spectrum for Ultra-WideBand (UWB) communications in ways to not cause interference on conventional Narrowband transmissions, but which limit UWB usage to short-range applications [1]. UWB is now being researched for a vast number of civilian, industrial and military applications: biomedical imaging devices [2], through-wall and ground mapping, short-range high bitrate transceivers, centimetre-precision radar [3] and automotive collision avoidance systems. These benefit from a virtually undetectable communication channel to Narrowband receivers as UWB pulses have a Power Spectral Density which covers a large range of frequencies and consequently falls below typical thermal noise levels.

Notwithstanding, UWB technology is still mostly based on custom ASIC solutions. This work focussed on developing and testing an Ultra-WideBand (UWB) system in programmable logic (FPGA), making UWB technology more affordable and more accessible to a broader audience. The result will be a short range IR-UWB communications device that can perform ranging measurements and also operate as a transceiver.

II. UWB definition

UWB differs from Narrowband radio as information is transmitted through narrow pulses, resulting in a large bandwidth usage. The FCC and ITU-R define UWB signals in terms of its bandwidth when transmitted from an UWB antenna. Signals with an absolute bandwidth greater than $500\,\mathrm{MHz}$ or which fractional bandwidth ratio is at least 0.20 are considered UWB (see Equation 1, where: $f_c = (f_H + f_L)/2$) [1].

$$f_{BW} = \frac{(f_H - f_L)}{f_c} \tag{1}$$

If baseband pulses do not comply with the minimum $500\,\mathrm{MHz}$ bandwidth, two alternatives to generate acceptable pulses are the *Switch-based* and *Up-conversion* methods. In the Switch-based solution a baseband signal switches the pulse generator oscillator on/off. Alternatively, in the Up-conversion method the baseband signal is up-converted to an upper central frequency. Therefore, signals can be carrier-free or carrier-based. There are also different ways of generating UWB signals: Impulse-Radio Ultra-WideBand (IR-UWB), Muti-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) and Frequency Modulation Ultra-Wideband (FM-UWB).

III. Single-Band or Impulse-based (IR-UWB)

IR-UWB signals typically consist of a sequence of short pulses under $2\,\mathrm{ns}$, modulated with Pulse-Amplitude Modulation (PAM), On-Off Keying (OOK), Pulse-Shape Modulation (PSM), Pulse-Position Modulation (PPM), Pulse-Width Modulation (PWM) or Binary Phase-Shift Keying (BPSK). Regarding Medium Access Control, *Time-Hopping* (TH) or *Direct-Sequence* (DS) techniques can enable band sharing without RF channel isolation. TH varies the position in time of transmitted pulses in relation to a known Pseudorandom Noise (PN) code. DS converts a PN sequence to several modulated pulses, forming a unique *chip*. This work uses a DS approach, making use of PN codes with appropriate cross-correlation and autocorrelation properties such as Gold and Kasami codes.

A. CTBV Signal Processing & DS Detection

The Continuous-Time Binary Value (CTBV) technique [4] consists on implementing a chain that performs continuous 1-bit threshold sampling and serial propagation of the binary value at the input to several correlators of a Rake Receiver logic circuit. A Rake Receiver performs correlations between its input signal and a sufficient number of delayed versions of the expected *chips*. The Rake topology is resilient to the effects of multipath propagation and fading. No clocked sampling is used between CTBV elements, the propagation takes place at the intrinsic speed of the CMOS logic gates. The length of the CTBV chain should accommodate the pulses of at least one entire *chip*, and the propagation delay of the logic elements should be significantly lower than the pulse length (τ_{pulse}).

IV. System Architecture

A. Transmitter Module Architecture

In order to generate a CTBV output, the FPGA's TX module is formed by a chain of *XORs* with delay buffers in between them. Polynomial coefficients of the *chip* to be transmitted are loaded in the chain and the pulses begin to propagate to the

* E-mail: costa.tiago@fe.up.pt
† Supervisor Professor, DEEC-FEUP. E-mail: sergio@fe.up.pt
‡ Second Supervisor Professor, DEEC-FEUP. E-mail: jca@fe.up.pt

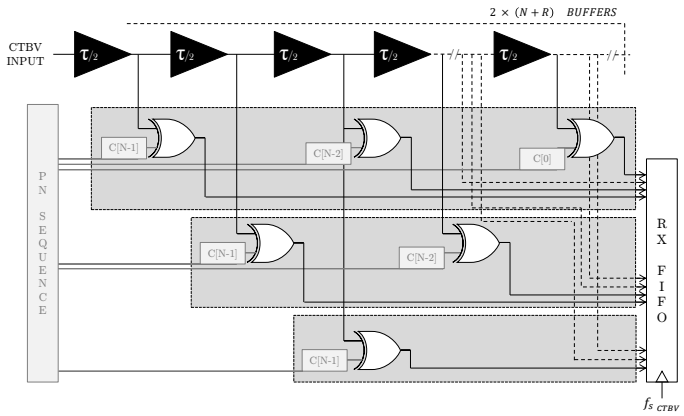

Fig. 1. Functional Block Diagram of the RX Module Architecture. A $\tau/2$ buffer represents a delay chain. The CTBV signal is propagated from the input through the chain and through *R* Rake correlators or fingers. The output of the correlators is stored in the RX FIFO module and later analysed for Gold or Kasami code identification.

CTBV output. The *XOR* chain requires a generator polynomial that can be obtained with a *XOR* operation between shifted versions of the desired PN code.

B. Receiver Module Architecture

The RX module contains *R* correlators, made of *XOR* primitives, that tap into the CTBV delay line at $\tau_{pulse}/2$, increasing the changes of synchronization and code detection (see Figure 1). The corresponding bit of the PN sequence to be detected is loaded on their second input. The output of every *XOR* in a given correlator will be logic *0* if all the inputs are aligned with the expected code. The opposite scenario can be used to detect an inverted code: if the *XOR* sum is equal to *N*, the code length, all inputs are misaligned. This property enables the detection of two different *chips* with the same receiver module, saving resources on programmable logic implementations.

C. Delay Buffer Architecture

The delay chain is composed of simple logic elements that are synthesizable from the Verilog primitive *wire*. The number of elements in each delay buffer varies with the desired bandwidth of the IR-UWB pulses, but there are some practical limits in FPGAs caused by the maximum internal propagation speed of logic signals, the maximum switching rate of I/O pins and the Place & Route process.

V. Proof-of-concept demonstrations

Ranging and Transceiver applications were implemented in the Altera Cyclone II family, model EP2C5T144C8N (see Table I).

A. Ranging Configuration

In wired mediums, ranging applications are made possible by the standing wave phenomenon observed in transmission lines, which results from impedance mismatching between a wave-guide and its load. By measuring the time difference between the instant when a *chip* was transmitted and the point of arrival after being reflected by the load, the Time of Flight (ToF) can be obtained. After the ToF is known, the distance of a transmission line can be estimated if the wave propagation velocity (v_P) of the medium is also known (see Equation 2).

TABLE I
Hardware Implementation Specification Overview [1]

Delay Elements	*K=4*	*K=8*	*K=12*	*K=16*
τ_{pulse}	3.3 ns	4.7 ns	6.0 ns	7.3 ns
τ_{chip}	50 ns	70 ns	90 ns	110 ns
Ranging Configuration				
Min. Load Distance	—	16.5m	21.3m	26.0m
Max. Load Distance	—	605m		
Max. Ranging Interval	—	5.12us		
Transceiver Configuration				
Payload bitrate	6.2 Mbit/s		5.5 Mbit/s	

(1) Valid for *N=15* and for a transmission line with a Velocity Factor of 0.788.

$$d_{Z_L} \approx v_P \cdot c_0 \times \tau_{ToF} \quad \text{(m)} \qquad (2)$$

B. Transceiver Configuration

The Transceiver configuration is a way of establishing bidirectional or multi-directional communication with identical systems by means of a CTBV IR-UWB transmission channel.

VI. Conclusion

The end result of this work was a simple, low-cost and easily re-configurable IR-UWB baseband generator and detector architecture for less complex next-generation IR-UWB systems. One of the main challenges encountered was guaranteeing that CTBV chains would offer constant propagation delays for precise pulse generation and detection. By using common Verilog primitives, it was actually possible to average out variable combinational logic delays. There are, however, limitations, as performance is still limited compared to ASIC UWB solutions.

Regarding future developments based on this implementation, the most relevant would be: deploying the architecture in more capable hardware and reaching *sub-nanosecond* measurement resolution; and also extending the design to the wireless domain, enabling radar measurements and IR-UWB wireless communications.

References

[1] F. C. Commission, "Revision of part 15 of the commission's rules regarding ultra-wideband transmission systems," FCC, Federal Communications Commission, Washington, D.C. 20554, FIRST REPORT AND ORDER ET Docket 98-153, mar 2002.

[2] M. Strackx, E. D'Agostino, P. Leroux, and P. Reynaert, "Direct rf subsampling receivers enabling impulse-based uwb signals for breast cancer detection," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 62, no. 2, pp. 144–148, Feb 2015.

[3] T. K. M. Md. Iqbal Hossain, "Distance measurement using ultra wideband," Masters Thesis, School of Technology and Health, Kungliga Tekniska Högskolan, feb 2012.

[4] S. Sudalaiyandi, H. Hjortland, T.-A. Vu, O. Naess, and T. Lande, "Continuous-time high-precision ir-uwb ranging-system in 90 nm cmos," in *Solid State Circuits Conference (A-SSCC), 2012 IEEE Asian*, Nov 2012, pp. 349–352.